

Anubhav Ammu

Linkedin: ammuanubhav

Github: anubhavammu2005-creator

Email: anubhavammu2005@gmail.com

Mobile: +91-6304834274

SKILLS

- **Languages:** Python, C, C++
- **Network Systems:** Computer Networks (EIGRP, RIP, VLANs), Routing & Switching
- **Tools/Platforms:** Verilog, Cisco Packet Tracer, Multisim, Git
- **Soft Skills:** Leadership, Collaboration, Problem Solving, Adaptability, Project Management, Diligent

TRAINING

Lovely Professional University

NextGen Networking - Summer Internship in Advanced Computer Networks: Jun'25 – Jul'25

- Worked on EIGRP configuration in a triangular topology using Cisco Packet Tracer.
- Hands-on experience in dynamic routing protocols, subnetting and router configuration.
- Enhanced troubleshooting skills using commands like ping, show ip route, and show running-config.

PROJECTS

Vending Machine Controller using Verilog HDL

Dec'25

- Created and implemented a **finite state machine (FSM)**-based vending machine using Verilog HDL, handling coin inputs, product selection, and state transitions.
- Developed modules for coin validation, balance calculation, product dispensing, and change return, ensuring correct transaction flow.
- Simulated and verified functionality using testbenches, covering edge cases such as insufficient balance and invalid inputs.
- Optimized logic for synchronous operation with clock and reset control, improving reliability and timing accuracy.

Multi-Level Switching using ASK (Amplitude Shift Keying)

Nov'25

- Implemented a **multi-level Amplitude Shift Keying (ASK)** scheme to transmit digital data using discrete amplitude levels.
- Built modulation and demodulation blocks to encode and decode **multiple bit levels per symbol**, improving data efficiency.
- Analyzed signal behavior under noise and channel variations through simulation.
- Compared performance metrics such as **bit error rate (BER)** and signal clarity for different amplitude levels.
- Gained practical understanding of **digital communication principles**, modulation techniques, and bandwidth–power trade-offs.

2-bit Digital Comparator Using CMOS and PTL

Mar'25

- Designed and simulated a 2-bit comparator using CMOS and PTL.
- Compared performance, power efficiency, and transistor count between CMOS and PTL.
- Applied design to understand low-power VLSI concepts.
- Analyzed **delay and power trade-offs** to highlight advantages of PTL over conventional CMOS.

CERTIFICATES

- System Design using Verilog Jan'26
- Database Management Systems (NPTEL) Dec'25
- Advanced Computer Networks, NextGen Networking (LPU) Jul'25

EDUCATION

- **Lovely Professional University** Punjab, India
Bachelor of Technology - Electronics and Communication Engineering Aug'23 – Present
- **Aditya Junior College** Andhra Pradesh, India
Intermediate; CGPA: 7.5 Jun'21 – Mar'23
- **Keshava Reddy Smart School** Andhra Pradesh, India
SSC; GPA: 10 Jul'20 – May'21